REMARKS

Claims 1-12, 14-46 and 48-63 remain pending in the application.

Allowed Claims

The Applicants thank the Examiner for the indication that claims 8-12, 18-28, 42-46 and 48-63 are allowed.

Objection to Claim 36

Claim 36 was objected to for alleged informalities.

Claim 36 is amended herein to correct any informalities. The Applicants respectfully request the objection to claim 36 be withdrawn.

Claims 1-3, 5, 6, 14, 16, 29-38 and 40 over Rich

In the Office Action, claims 1-3, 5, 6, 14, 16, 29-38 and 40 were rejected under 35 U.S.C. §102(b) as allegedly being anticipated by U.S. Pat. No. 5,784,370 to Rich ("Rich"). The Applicants respectfully traverse the rejection.

Claims 1-3, 5, 6, 29-38 and 40 recite a method and apparatus utilizing parallel communications channels connecting a PLD to an LLD, with control signals being sent from the PLD to the LLD out-of-band from information signals.

Rich appears to disclose an extender circuit that provides a serial communication interface between an ATM layer and a PHY layer (Abstract). An ATM interface is comprised of a parallel interface circuit and serial interface circuit (Rich, Fig. 3). The ATM serial interface circuit communicates with the PHY serial interface circuit through a **serial communication path** (Rich, Fig. 3).

The Examiner had previously acknowledged that Rich fails to disclose an out-of-band channel for control signal (see Office Action, dated March 13, 2003). However, the Examiner now points to Rich, items 1382-1358 and 1364-1386 to disclose channels that communicate control signals out-of-band from information signals (see Office Action, page 3).

Channels 1382+1358 and 1364+1386 are simply various types of information lines throughout Rich's ATM **serial interface circuit**, **NOT** connecting Rich's ATM layer **to** the PHY layer. The parallel communication channels connect the various components **within** the serial interface circuit do **NOT** connect the ATM layer **to** the PHY layer, as alleged by the Examiner. The actual connection between the ATM layer and a PHY layer is a **serial communication channel**. Thus, a **single** serial communication channel is **NOT** parallel communications channels connecting a PLD to an LLD, with control signals being sent from the PLD to the LLD out-of-band from information signals, as recited by claims 1-3, 5, 6, 29-38 and 40.

Moreover, claims 1-3, 5 and 6 recite a physical layer device (PLD) **comprising** a PLD send interface including PLD parallel information outputs and at least one PLD control output; and a logical link device (LLD) **comprising** an LLD receive interface including LLD parallel information inputs and at least one LLD control input.

Rich's Fig. 2 shows a high level view of interface 206 between an ATM layer and a physical layer 204. Fig. 13 shows a lower level view of an interface between an ATM layer and a physical layer as shown in Fig. 2 with ATM layer 1302 and physical layer 1304 being **distinct elements** from items 1316, 1320, 1384, 1386, 1306, 1310, 1358 and 1362. Rich fails to disclose or suggest a physical layer device (PLD) **comprising** a PLD send interface including PLD parallel information outputs and at least one PLD control output; and a logical link device (LLD) **comprising** an LLD receive interface including LLD parallel information inputs and at least one LLD control input, as recited by claims 1-3, 5, 6, 14, 16, 29-38 and 40.

Moreover, even if Rich's physical layer device 1304 comprises items 1316, 1320, 1384 and 1386, and logical layer 1302 comprises items 1306, 1310, 1358 and 1362, which as discussed above **they do not**, Rich utilizes **serial paths 1328 and 1330** to connect the ATM layer and PHY layers, **NOT parallel information paths**, as recited by claims 1-3, 5 and 6.

Rich's interface circuit comprising a PLD send interface including PLD **serial** information outputs; and a logical link device (LLD) comprising an LLD receive interface including LLD **serial** information inputs is **NOT** a physical layer device (PLD) comprising a PLD send interface including PLD **parallel information outputs** and at least one PLD control output; and a logical link device (LLD) comprising an LLD receive interface including LLD **parallel information inputs** and at least one LLD control input, as recited by claims 1-3, 5 and 6.

Accordingly, for at least all the above reasons, claims 1-3, 5, 6, 14, 16, 29-38 and 40 are patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Claims 4, 15 and 39 over Rich in view of AAPA

In the Office Action, claims 4, 15 and 39 were rejected under 35 U.S.C. §103(a) as allegedly being obvious over Rich in view of Applicant's Admitted Prior Art ("AAPA"). The Applicants respectfully traverse the rejection.

Claims 4 and 15 are dependent on claims 3 and 14, and are allowable for at least the same reasons as claims 3 and 14.

Claims 4, 15 and 39 recite a method and apparatus utilizing parallel communications channels connecting a PLD to an LLD, with control signals being sent from the PLD to the LLD out-of-band from information signals.

As discussed above, Rich fails to disclose or suggest a method and an apparatus utilizing parallel communications channels connecting a PLD to an LLD, with control signals being sent from the PLD to the LLD out-of-band from information signals, as recited by claims 4 and 15.

The Examiner relies on AAPA to allegedly disclose symmetrical interfaces as disclosed on page 23 of the Applicant's specification (Office Action, page 7). However, page 23 of the Applicant's specification is part of the "Detailed Description of the Preferred Embodiments", **NOT** part of AAPA that ends on page 8 of the specification.

Accordingly, for at least all the above reasons, claims 4, 15 and 39 are patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Claims 7, 17 and 41 over Rich in view of Akata

In the Office Action, claims 7, 17 and 41 were rejected under 35 U.S.C. §103(a) as allegedly being obvious over Rich in view of U.S. Pat. No. 5,594,724 to Akata et al. ("Akata"). The Applicants respectfully traverse the rejection.

Claims 7 and 41 recite a method and an apparatus utilizing parallel communications channels connecting a PLD to an LLD, with control signals being sent from the PLD to the LLD out-of-band from information signals.

As discussed above, Rich discloses a **distinct** interface circuit connecting a PLD to an ATM over a serial connection. Rich fails to disclose or suggest a method and an apparatus utilizing **parallel communications channels** connecting a PLD to an LLD, with control signals being sent from the PLD to the LLD out-of-band from information signals, as recited by claims 7 and 41.

Akata is relied on by the Examiner to disclose a SONET and a SDH device, wherein an SDH generating section can interface with an ATM system in order to reduce the hardware amount by causing a plurality of paths to share a circuit for generating or terminating a TC layer (Office Action, page 8). However, as the Examiner acknowledges, Akata fails to disclose or suggest a method and an apparatus utilizing parallel communications channels connecting a PLD to an LLD, with control signals being sent from the PLD to the LLD out-of-band from information signals, as recited by claims 7 and 41.

Neither Rich nor Akata, either alone or in combination, disclose, teach or suggest a method and an apparatus utilizing parallel communications channels connecting a PLD to an LLD, with control signals being sent from the PLD to the LLD out-of-band from information signals, as recited by claims 7 and 41.

Claim 17 is dependent on claim 14, and is allowable for at least the same reasons as claim 14.

Claims 7, 17 and 41 recite a physical layer device (PLD) **comprising** a PLD send interface including PLD parallel information outputs and at least one PLD control output; and a logical link device (LLD) **comprising** an LLD receive interface including LLD parallel information inputs and at least one LLD control input.

As discussed above, Rich fails to disclose or suggest a physical layer device (PLD) **comprising** a PLD send interface including PLD **parallel** information outputs and at least one PLD control output; and a logical link device (LLD) **comprising** an LLD receive interface including LLD **parallel** information inputs and at least one LLD control input, as recited by claims 7, 17 and 41.

Akata fails to even mention the types of connects used between the components throughout the system, not mentioning parallel communication channels for any purpose. Akata fails to disclose or suggest a physical layer device (PLD) **comprising** a PLD send interface including PLD parallel information outputs and at least one PLD control output; and a logical link device (LLD) **comprising** an LLD receive interface including LLD parallel information inputs and at least one LLD control input, as recited by claims 7, 17 and 41.

Neither Rich nor Akata, either alone or in combination, disclose, teach or suggest a physical layer device (PLD) **comprising** a PLD send interface including PLD parallel information outputs and at least one PLD control output; and a logical link device (LLD) **comprising** an LLD receive interface including LLD parallel information inputs and at least one LLD control input, as recited by claims 7, 17 and 41.

Accordingly, for at least all the above reasons, claims 7, 17 and 41 are patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Conclusion

All objections and rejections having been addressed, it is respectfully submitted that the subject application is in condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,
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